MOORE'S LAW SCALING AND RADIATION EFFECTS IN MOS DEVICES

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Microelectronic devices and ICs experience high radiation levels in space, defense, and particle accelerator environments. After the invention of the transistor in 1947 [1], radiation effects research focused primarily on defect creation in semiconductor materials and displacement damage in bipolar junction transistors [2]–[5]. The sensitivity of MOS transistors to total ionizing dose (TID) effects was discovered by Hughes and Giroux in 1964 [6], just one year before Moore's law was postulated [7], [8]. An early and influential study of TID effects in MOS devices was co-authored in 1967 by a young Andy Grove, while still at Fairchild Semiconductor [9], [10]. The modern era of radiation-tolerant MOS electronics began in 1971 with the development of radiation-hardened *p*MOS technology by Hughes Aircraft Company [8], [11].

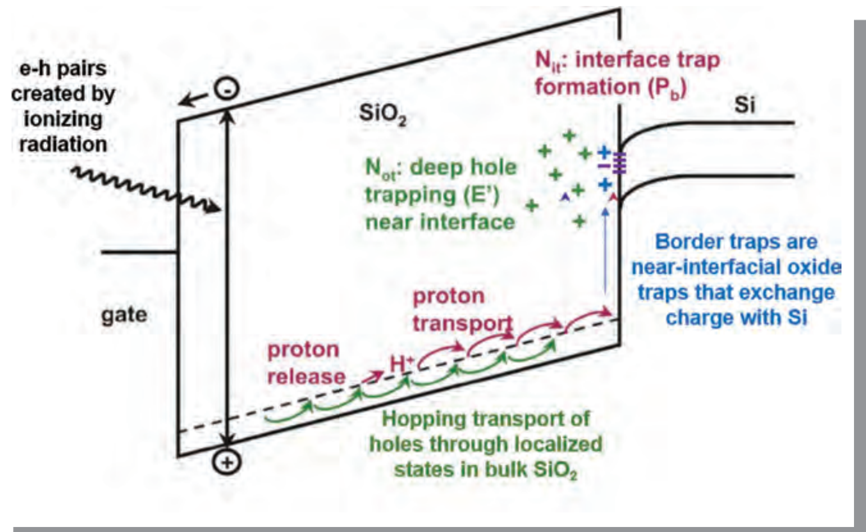

Figure 1. Schematic illustration of electron-hole pair generation, charge transport, and trapping in irradiated MOS devices. (After [8], [12], [13].)

Fig. 1 illustrates the chain of events that occur during and after TID-irradiation of MOS devices [8], [12], [13]. Primary effects include hole transport and trapping in gate and isolation oxides and buildup of interface and border traps at or near gate-dielectric/semiconductor boundaries. Proton (H^+) release during hole transport and field-induced H^+ transport to the Si/SiO_2 interface play critical roles in interface and border-trap formation [8], [12], [13].

Moore's Law scaling and changes in device architecture significantly affect MOS radiation response [10], [14]–[17]. Progressively thinner gate and isolation oxides in highly scaled devices (Fig. 2) generally lead to enhanced TID tolerance (Fig. 3). However, in current and future generation FinFETs (Fig. 2(c)), gate-all-around, and nanosheet or forksheet devices, the thickness and quality of the gate insulator and isolation oxides, transistor channel/edge doping levels, and strength of gate control all strongly affect charge trapping [10], [14]–[17]. Thus, significant variations are expected and observed in the TID response of MOS devices and ICs [10], [16].

As MOS technologies have evolved and device dimensions and operating voltages have decreased, single-event effects (SEE) due to cosmic rays and/or high-energy protons have become an increasing concern. When a single high-energy charged particle deposits a sufficient amount of energy per unit path length to generate a densely ionized track, soft or hard errors can result, with probabilities determined by the amount of collected charge and resulting device/IC response [10], [16], [18]–[20]. Until the ~130 nm technology node, SEE in electronics in space environments typically increased with decreasing feature size, as seen in Figs. 4 and 5. This is due primarily to reductions in operating voltage and critical charge to upset [10], [16], [18]–[20]. Fortunately, Moore's Law scaling greatly enhances design, layout, modeling, and simulation capabilities, which are increasingly necessary to understand and mitigate the resulting effects [14], [16], [18].

By the mid-1990s, device scaling made terrestrial electronics sensitive to soft errors caused by reactions of atmospheric neutrons in silicon and surrounding materials [21], [22]. Removing B_{10} from processing and changing to FinFET/Tri-Gate

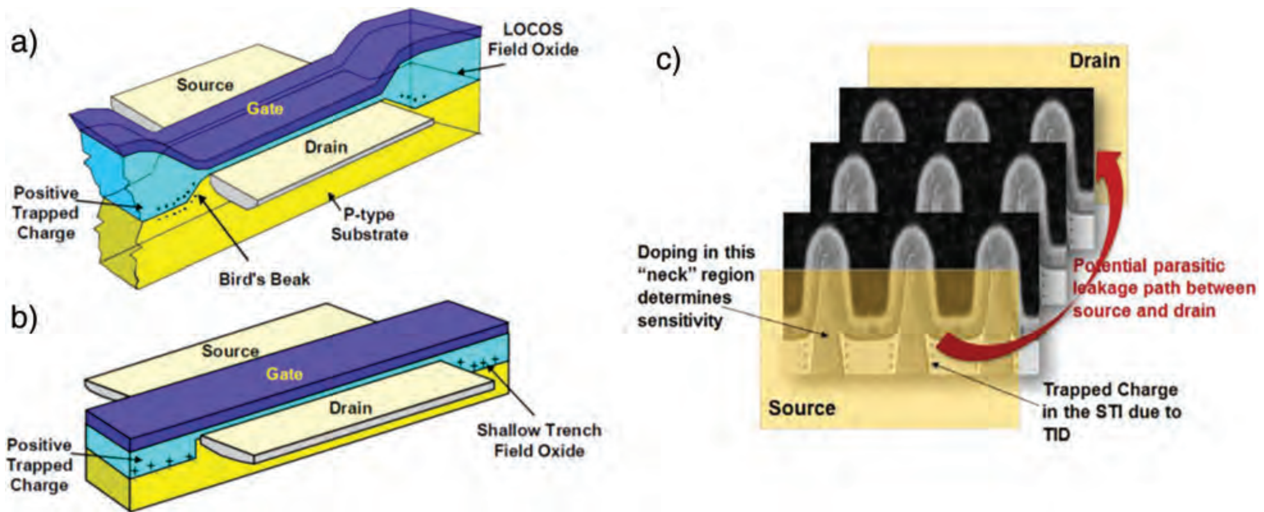

Figure 2. MOS devices with (a) LOCOS (local oxidation of silicon) or (b) shallow-trench isolation, STI [15]. (c) Bulk FinFETs [17].

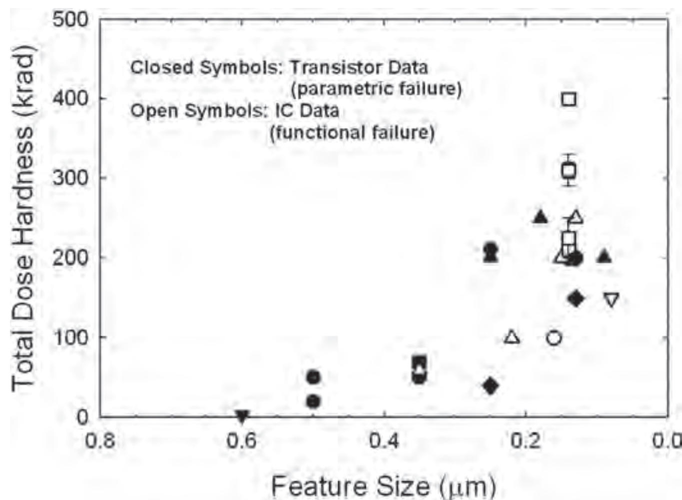

Figure 3. Hardness of MOS ICs to TID vs. feature size. (After [16].)

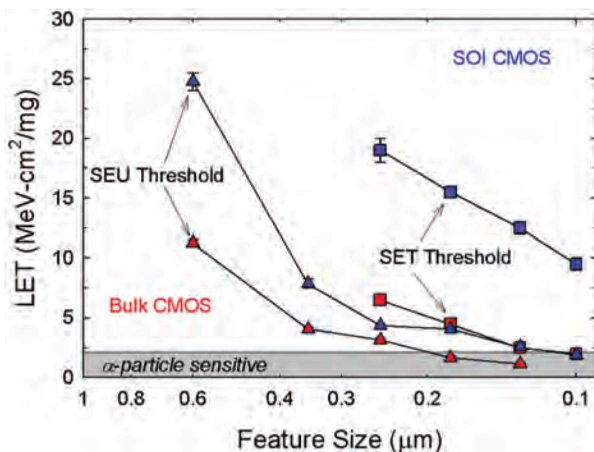

Figure 4. Critical ion LET (linear energy transfer) to failure vs. feature size for planar bulk and SOI (silicon on insulator) CMOS ICs. The buried oxide layer makes SOI devices less sensitive to SEE. (After [16].)

architecture (Fig. 5, inset) can greatly reduce SERs in ICs [19], [22]. However, as transistor sensitive volumes become smaller than ion tracks and transistor packing densities continue to increase, multiple-bit errors and "charge sharing" among adjacent devices become more significant [10], [16], [18]. ICs now are more three-dimensional, and nanoscale MOS devices can be sensitive to single-particle displacement damage [10], [23]. Thus, each new IC technology generation continues to present new radiation-effects challenges.

Biography

Dan Fleetwood received his Ph.D. from Purdue University in 1984. He joined Sandia National Laboratories in 1984 and was named a Distinguished Member of Technical Staff in 1990. Dan joined Vanderbilt University as a Professor of Electrical Engineering in 1999. From 2003–2020 he chaired Vanderbilt's EECS Department; since 2009 he has been appointed Olin H. Landreth Chair in Engineering. He received the 2009 IEEE Nuclear and Plasma Sciences Merit Award, and is a Fellow of IEEE, AAAS, and the American Physical

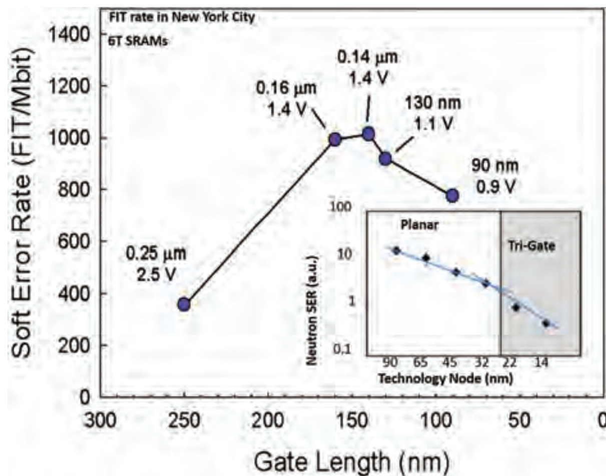

Figure 5. Feature size dependence of terrestrial-neutron soft-error rates (SER) in bulk planar six-transistor static RAMs and (inset) tri-gate (FinFET) CMOS ICs. One FIT = one failure in 10^9 h. (After [16], [22].)

Society. His research interests include radiation effects on microelectronics, low-frequency noise, and defects in microelectronic materials and devices.

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